

Triple Output Regulator with Single Synchronous Buck and Dual LDO

The ISL6415 is a highly integrated triple output regulator which provides a single chip solution for wireless chipset power management. The device integrates a high efficiency synchronous buck regulator with two ultra low noise LDO regulators. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.2V (PWM), 1.8V (LDO1), and another ultra-clean 1.8V (LDO2).

The Synchronous current mode PWM regulator with integrated N- and P- channel power MOSFET provides pre-set 1.2V for BBP/MAC core supply. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The ISL6415 also has two LDO regulators which use an internal PMOS transistor as the pass device. LDO2 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6415 also integrates a RESET function, which eliminates the need for additional RESET IC required in WLAN applications. The IC asserts a RESET signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after VIN has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include overcurrent protection for all three outputs and thermal shutdown.

High integration and the thin Quad Flat No-lead (QFN) package makes ISL6415 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

Ordering Information

PART NUMBER*	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6415IR	-40 to 85	24 Ld QFN	L24.4x4B
ISL6415IRZ (Note)	-40 to 85	24 Ld QFN (Pb-free)	L24.4x4B

*For tape and reel, add "-TK" or "-T5K" suffix.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Fully Integrated Synchronous Buck Regulator + Dual LDO
- High Output Current (For QFN package)
 - PWM, 1.2V 400mA
 - LDO1, 1.8V 300mA
 - LDO2, 1.8V 200mA
- Ultra-Compact DC-DC Converter Design
- Stable with Small Ceramic Output Capacitors
- High Conversion Efficiency
- Low Shutdown Supply Current
- Ultra-Low Dropout Voltage for LDOs
 - LDO1, 1.8V 125mV (typ.) at 300mA
 - LDO2, 1.8V 100mV (typ.) at 200mA
- Ultra-Low Output Voltage Noise
 - <30µV_{RMS} (typ.) for LDO2 (VCO Supply)
- PG_LDO, PG_PWM and $\overline{\text{PG_PWM}}$ outputs
- Extensive Circuit Protection and Monitoring Features
 - Overvoltage protection
 - Overcurrent protection
 - Shutdown
 - Thermal Shutdown
- Integrated RESET output for microprocessor reset
- Proven Reference Design for Total WLAN System Solution
- QFN Package
 - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
 - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile
- Pb-Free Available (RoHS Compliant)

Applications

- WLAN Cards
 - PCMCIA, Cardbus-32, Mini-PCI Cards
 - Compact Flash Cards
- Liberty Chipset
- Hand-Held Instruments

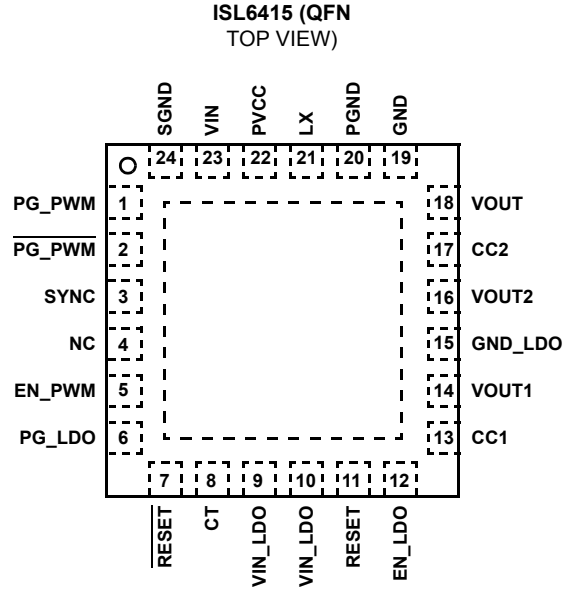
Related Literature

- TB363 - Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)
- TB389 - PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

Final pinout and specifications are subject to change.

ISL6415

Pinout



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